Performance Analysis of various Parameters of Network-on-chip (NoC) for different Topologies

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ABSTRACT: Network on a chip is a concept in which a single silicon chip is used to implement the communication features of large-scale to very large-scale integration systems. For high-end System on Chip designs, Network on Chip is considered the best integrated solution. NoC has several advantages over dedicated wiring and buses i.e. increased bandwidth, low latency, less power consumption and scalability. Reduction in the latency (end-to-end latency and network latency), loss probability, energy consumption and response time are the basic parameters which are considered by the researchers for the optimization of the networks-on-chip topologies. In this paper we review the most popular technologies and also some recent topologies for interconnection networks. We study their performance and summarize their strengths & weakness.

KEYWORDS: System on Chip, Network on Chip, Optimization, Topologies

1. INTRODUCTION:

Networks-on-chip (NoCs) has become an alternative to the conventional System on Chip SoC [2]. It is an improved concept to reduce the communication gap between multi -core (SoC). In NoC, design of Topologies plays a very vital role. Parameters which improve the performance of the networks are throughput, injection rate, latency, minimum chip area and hop counts [3]. For smooth and efficient communication between the IPs (Intellectual Properties) NoC play a vital role. Different topologies are designed and classified on basis of parameters like hop counts, throughput, latency, injection rates. Comparative study of different topologies will explore some new advancement in Network on Chip design.

1.1 Mesh Topology

Researchers use Mesh Topology as one of the most basic topology in NoC design. It is a type of direct topology where there is direct connections among the nodes [1]. It provides high path diversity and also improves scalability. Mesh topology was designed basically for military applications but currently they are used in smart buildings, home automation and multimedia processing. All nodes share the data among each other. It has multiple sources to destination routes and an efficient addressing scheme which avoids any disturbance in networks. All nodes are connected in the form of 2D lattice [2] and adjacent nodes are connected to each other. Inter-switch delays and robustness in the network can be avoided in mesh topology.

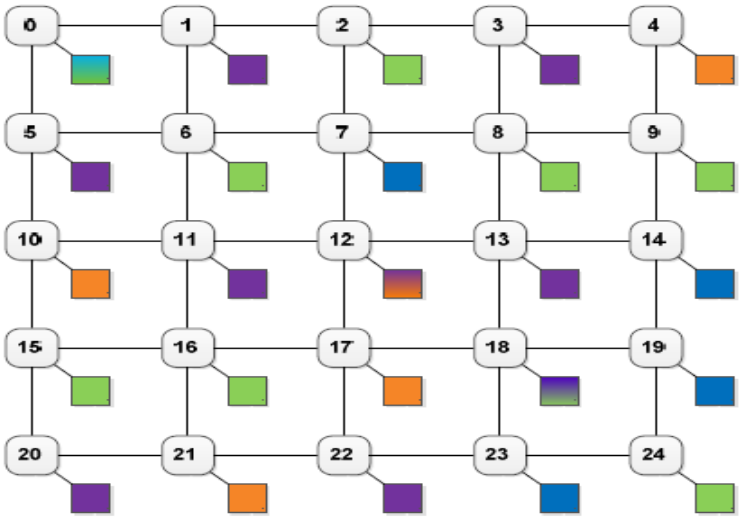

Figure 1: Mesh Topology

1.2 Torus Topology

Torus topology is an extended version of Mesh Topology. It is an example of direct topology. It differs from Mesh topology in such a way that each column head connects to tail of the same column and leftmost node of every row is connected to the right end corner node of every column. The main advantage of this topology is that it can have improved diversity in path as its geometry is symmetric in edge also it has low hop-count H. Main disadvantage of this network is that as the length of wire increases in joining nodes in both rows and columns there is increase in latency [4].

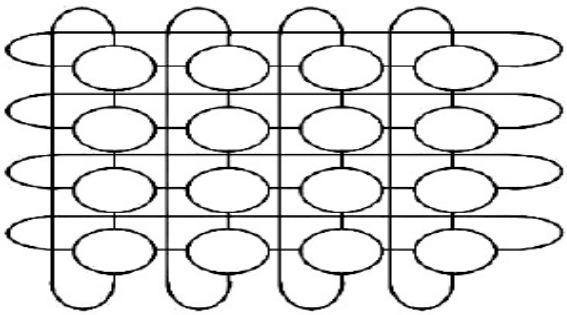

Figure 2: Torus Topology

1.3 Ring Topology

Ring topology is a type of network in which a circular path is created to transfer data among the nodes. It is a one directional ring network in which packets travel only in one direction. It is considered as one of the popular topology. Every adjacent node is connected with single wire hence each node has two adjacent neighbours as shown in figure 3. Equal bandwidth is distributed to each node hence in Ring topology degree of every node is two. The short comes of this topology is that if there is break in single cable breakdown occurs

in the whole network and as a result expansion of network reduces the performance of the entire network. The data travels through each node in the ring till it reaches the destination node [5]

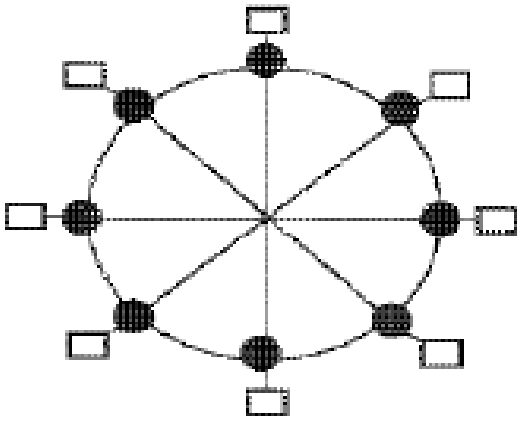

Figure 3: Ring Topology

1.4 Star Topology

This topology is simplest among all other existing topologies in terms of its construction. It is a topology used for LAN (Local Area Connection) connection in which all nodes are connected to a central point just like a hub. This topology requires more cable as compared to other conventional topologies. The main short come of this topology is that if the central node fails then there is breakdown in the entire network. As the number of adjacent nodes connected to central node increases there is hike in its diameter [4].

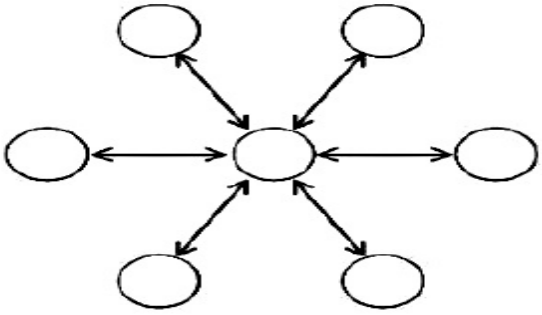

Figure 4: Star Topology

1.5 Butterfly Topology

This topology links many computers to a very high speed networks. Processor nodes, Router and links are the major components of this topology. The connection of nodes is as shown in figure 5. Bisection band-width, degree and diameter are the network parameters considered in butterfly topology design and imple-mentation.

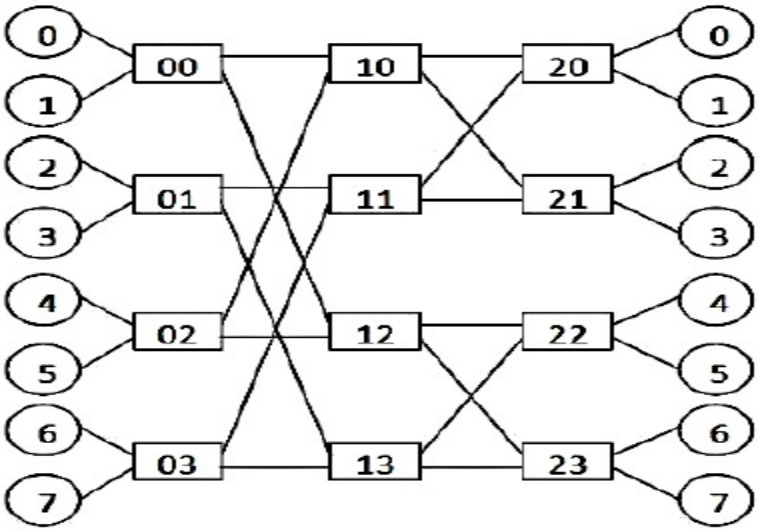

Figure 5: Butterfly Topology

1.6 Routing Algorithms

It maps the path of the packets which it has travelled from source end to destination end.

1.7 Flow Control

The flow control monitors allocation of flits, Virtual Channels (VC) buffers and clients.

2 LITERATURE SURVEY

All major topologies and parameters used in NoC designs have been briefed.

Suchi Johari et.al [1] developed a modified Mesh Topology called HHCT (heterogeneous and hybrid clustered topology). Communication among the various cores had been made possible. The geometry of the proposed topology has been kept constant with Mesh topology which helps to keep design area constant. The advantage of proposed topology is reduction in hop counts among different cores which also reduces energy consumption, latency, sink bandwidth and loss probability. The performance of HHCT NoC as compared to Mesh topology has improved to a great extent as the cores in NoC are clustered.

Wang Zhang et.al [2] proposed architecture along with 2 dimension Mesh topology, odd-even routing algorithm, input buffers and wormhole switching technique. The odd even routing algorithm is a type of Adaptive Routing Algorithm. The proposed architecture is evaluated by using NIRGAM Simulator. Busty traffic and CBR (Constant Bit Rate) techniques are considered for simulation purpose. The network architecture is optimized using proposed NoC architecture.

Alakesh Kalita et.al [4] developed a distinct topology without changing factors as like reduced chip size, maximum throughput and low latency. Proposed topology has been compared with Multipath and Fat tree topology considering hop-counts, latency in the simulation software. Future work lays in making proposed topology a fault liberal topology with reduced end-to-end latency. Reduction in number of hops is the main advantage of proposed topology.

Nikhil baby et.al [6] compared Torus, 2D Mesh and RiCoBit topologies. The parameters used for comparison are time consumption, number of nodes used and path traversed. To develop an advanced processor and improve performance of the systems is the ultimate aim of proposed RiCoBit topology.

Abhijit Biswas et.al [7] proposed design of MIN Fat Tree Topology. The congestion related to internal routers has been reduced by creating additional link amongst each router. Hop count as well as average delay shows excellent results after comparing with MIN FAT Tree topology. Proposed topology exhibits better result as compared with conventional topologies.

Kaushik Ray et.al [9] proposed an advanced topology which exhibits path diversity and improved degree of scalability. Adaptive routing algorithm has been utilized for implementation. Simulation part has shown excellent results when compared with Fat tree topology in terms of number of events and average latency. Also chip are has been reduced as this topology uses switches to a very small extent. The proposed topology exhibits better result compared with existing topologies.

A.Yu.Romanov et.al [10] proposed realization of Circulant topologies and compared its mathematical side as well as advantages with hypercube, torus and mesh topologies. The developed software is also compared with widespread regular existing topologies in accordance with area distance among nodes as well as diameter.

Dhawani P. Sametriya et.al [11] studied a general comparison between HC-CPSoC and CPSoC architecture. Also elaborated CPSoC structure along with its components. HC-CPSoC shows better results as compared to CPSoC. Also development of 3D-stacking as well as designing of Network on Chip in terms of 3D CPSoC is done as future research work. Routing Algorithm which is cluster based is implemented for CPSoC.

Jiechen Zhao et.al [12] focused on ONoC (Optical Network on Chip) architecture which provides minimum latency and very less bandwidth for chip design. The communication among two nodes is made possible by implementing a 3D-DMNoC architecture which requires very less amount of resources. Improved simulation parameters in terms of throughput as well as delay are shown in simulation results.

P.Veda Bhanu et.al [13] developed an advanced NoC interconnection concept. A novel BFT (Butterfly fat tree) network which is used to assign faults in network is also designed. By using BFT topology system performance is surged in accordance with parameters like power consumption, cost and size of the network. Also the comparison between ILP (Integer Linear Programming) and PSO (Particle Swarm Optimisation) has been implemented in this paper.

L.Mourelle et.al [14] executed migration plan of action for parallel genetic algorithms in MPSoC (multiprocessor system-on-chip).This can help parallel processing techniques like internet of things as well as mul-

timedia. Also two advanced migration plans are suggested to improve the efficiency of the system. Detail classification regarding Ring Topology and Neighbourhood Topology has been implemented.

R.K.Jena et.al [15] addressed the short comings of topological mapping of IPs by using multi objective evolutionary algorithm. Main objectives considered in this topology are bandwidth requirements of the link and consumption of energy. Productiveness and precision of the implemented model is evaluated. Energy consumption and bandwidth requirements have been minimized dealing with some of existing topologies.

Md.Hasan Furhad et.al [16] proposed ScMesh (shortly connected mesh technology) and compared it with conventional Mesh Topology. Reduction in entire network diameter, minimum chip design area and low power improves network performance. Simulation result shows better performance of ScMesh topology in comparison with Butterfly fat tree, WK- recursive and allied topologies. Also improvement in energy consumption, area overhead and latency is additional advantage of ScMesh topology.

Muhammad Rehan Yahya et.al [17] proposed the new concept of ONoC Optical network on chip which is an advanced concept to satisfy the requirements of many core processors. Along with electrical properties the Optical properties are also considered and compared with Torus and Mesh topologies. For greater packet sizes ONoC has shown excellent simulation results in terms of latency and throughput. Also advanced routing algorithm has been developed for hybrid network to minimise the latency in terms of a multi processor system.

Na Niu et.al [18] proposed a novel algorithm for 2D REmesh Networks-on-Chip. This advanced backtracking algorithm supports the uneven topologies produced due to damaged cores without changing the actual structure of the topology. The performance of the system has been evaluated by means of appropriate simulation software. The proposed algorithm is compared with TRARE algorithm.

N.L. Venkataraman et.al [19] developed a modified algorithm for buffer less routing NoC. ALO (Anti Lion Optimised) topology has also been introduced which offers very less power in NoC. For design and implementation of the proposed work XILINX ISE tool is being used to validate the simulation results. Anti Lion topology results have been compared with existing topology in terms of speed and power consumption.

Akram Reza et.al [21] studied photonic networks in details. An advanced topology which helps to curb insertion loss is being proposed. By using appropriate simulation tools analysis of proposed topology for real time and synthetic applications. Using more wavelength channels by decreasing the insertion loss improves performance of the system in terms of bandwidth and latency.

M. M. Hafizur Rahman [22] constructed a (HMMN) (Horizontal Midimew connected Mesh Network) topology. The simulation result shows that HMMN shows better results as compared to other conventional topol-

ogies. The communication between static and dynamic network shows improvement. Evaluation of message traffic, cost factor of HMMN is compared with conventional topologies. Also in terms of wrap cost and diameter HMMN outperforms torus topology. Design of parallel computer systems is possible in future by use of HMMN concept.

Sajed Dadashi et.al [23] proposed a "Balanced Mesh" topology which balances the connection among various segments of a Mesh network. Delay along with power consumption can be decreased of both delay and interposer layer without much change in degree of nodes. Efficiency of the system can be improved with less number of links as compared to C-Mesh and Butterdonut topologies. Betterment in latency as well as power consumption can be achieved with Balanced Mesh Topology.

3 RESEARCH GAP

Reference Paper	Topology used	Parameters	Remarks
Suchi Johari et.al [1]	Heterogeneous and Hybrid clustered topology (HHCT)	Latency, Response Time, Loss Probability, Injection rate	The number of hops are reduced due to which the Energy consumption, link utilization, loss probability, sink bandwidth is reduced.
Wang Zhang et.al [2]	2 Dimension Mesh Topology considering Constant Bit Rate (CBR) and Busty Traffic.	Average Latency per flit, Average Throughput	Mesh topology is considered as implementation of higher ordered topologies is quiet hard. The network performance of proposed NoC architecture is well optimized
Alakesh Kalita et.al [4]	New Topology for NoC with live lock free and deadlock algorithm	Chip area, Throughput, Latency, Hop counts, Scalability	The number of routers in the proposed topologies has reduced which results in low latency, high scalability and improved performance.
Nikhil baby et. Al [6]	Mesh, Torus and RiCoBit	Latency, Hops	RiCoBit topology has added advantages over Mesh & Torus topology in terms of number of

			nodes used and path traversed
Abhijit Biswas et.al [7]	MIN Fat Tree Topology	Delay, Congestion, Hop Counts	A bidirectional link is added to each router which is not present in conventional topologies which results in reduction of delay, hop counts and congestions
Dhawani P. Sametriya et.al [11]	CPSoC Hardware Topology (HC-CPSoC)	Overall throughput, Real time performance, QoS	HC-CPSoC shows better results as compared with CPSoC in terms of Chip size, cost, QoS, Real time performance and Overall throughput
Jiechen Zhao et. Al [12]	3D-DMONoC	Delay, throughput, area overhead and power consumption	3D-DMONoC possesses better results in terms of resources used, maintains low latency, improved throughput and delay.

4 CONCLUSION

Topologies play a major part in NoC Design. This paper explains different types of topologies like Ring, Mesh, Torus, Folded Torus, Fat tree etc. As the network grows, the conventional SoCs (System on Chip) which is bus based fails to scale. In this paper we reviewed some classic topologies and list their strength and shortcomings. The parameters which are considered while designing the architectures of topologies are Average Latency, Throughput, Injection rates, Hop counts etc. Also classification of various topologies is explained briefly in literature survey. The analytical modelling as well as cost of the topologies will be covered as the future work of this research. The recent topologies reviewed have not been really applied to practice but they bring opportunities for research area in NoC Router design.

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