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3D Torus Router Architecture For Efficient Network on Chip Design

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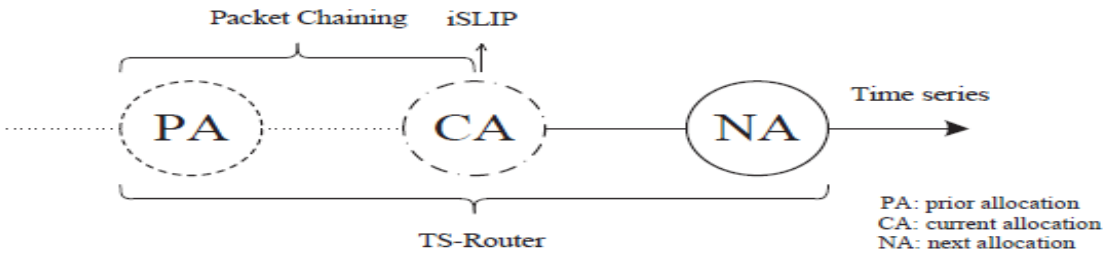
ABSTRACT: Network on Chips are becoming an important aspect in areas of multiprocessor chip design and high performance computing. Reduction in usage of excess amount of hardware in router design without operating all parameters can improve the performance of the system. The practical review of various routers applied in future of networking is carried out in this paper. Fundamental design considerations and various components involved in router design in terms of communication, energy management and power conversion is summarized in detail. A brief comparison of various routers designed previously has been made along with design aspects for 3D Torus router.

KEYWORDS: Network on Chips, High performance computing, adaptive routing algorithms, router, power conversion

I. INTRODUCTION:

Network on Chips (NoCs) is an important communication medium to connect various cores and associated modules of memories on chip [1]. A larger section of entire chip design is consumed by NoCs which increases the power expenses. The problem arises during scaling down of the transistor. Power reduction techniques thus plays a vital role in design of NoC routers in future. The main aim of communication system is transfer of data with maximum throughput and reduced latencies [3] by using less amount of resources. Switch Allocation (SA) is a crucial step in router design of NoCs [4] through which output ports are directly assigned to input ports.



ISSN: 0971-1260
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Figure1: Switch Allocation Strategies

- **Components used in Router Design:**

Router is a travelling path of packets from transmitting section to receiving section by hopping technique. The router is designed using hardware components like control logic, switches, I/O ports and buffers.

II. LITERATURE SURVEY

Hemanta Kumar Mondal et.al [1] designed a structured WNoC model using AMS (Adaptive Multi-Voltage Scaling) with no change in the performance of NoC router. Use of router architecture for different applications is being predicted and scaling of voltage is done with accordance. The proposed model reduces the consumed power by using power gating Wireless Interfaces (WIs) which are not part of actual communication.

Hao Zheng et.al [2] proposed EZ-pass (Easy pass) router architecture which reduces static power as well as high wake up latency. Ideal components in the network are used to transmit the packets without disturbing the actual router. Power Gating techniques are used to reduce network latency as well as static and dynamic power consumption in NoC router design.

Cunlu Li et.al [4] utilized RoBs (Reorder Buffers) which reduces the switch allocation problem in router design. RoBs helps to reduce the performance of the system by reducing blocking in HoL. An efficient RoB router is designed which manages the number of flits. RoB router uses minimum resources with reduced power consumption to improve performance of the system.

Authors proposed [5-8] a novel IMR (Isolated Multi ring) NoC that supports CMPs (Chip Multi Processors) design with higher cores. A Ring Topology is used as a base for IMR NoC design. IMR improves the performance of the network without actual using much hardware. Overall network latency and throughput of IMR is improved as compared with other existing topologies.

Ramon Fernandes et.al [10] designed OcNoC architecture whose design is based on Lasio NoC. It applies two approaches based on one cycle 3D Mesh Network on Chips. In comparison with existing routers there is improvement in application latency and network latency. Minimum silicon area is utilized in design of proposed model as compared with existing micro architectures of routers.

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

III. Router Architecture design for 3D Torus

The router design is based on credit based flow control strategy. It involves adaptive routing algorithm implementation that executes virtual cut using switching techniques. The router is designed to implement a new topology called as 3D Torus. It consists of 1 port which is connected at PE port and 6 ports which are connected to adjacent nodes [11-20]. The hardware parameters of 3D Torus are implemented on device like Xilinx Kinetic 7 and verified on Modelsim tool is listed as shown.

i. Buffer: Buffers are FIFO (First Input First Output) which stores flits as well as packets when output port remains busy.

ii. Routing Path Controller: It is used to implement adaptive routing algorithm and manages path to push forward the packets in assigned network.

iii. Virtual Channel Controller: It controls any deadlocks assigned in the system [11]. VCs are guided by adaptive routing algorithms which provide a fixed path for different packets arriving through various channels.

iv. Arbiter: Arbiter connects both input links with output links. It is tested for its fairness. Variable priority arbiter, Round robin and fixed concern arbiter are basic arbiters available.

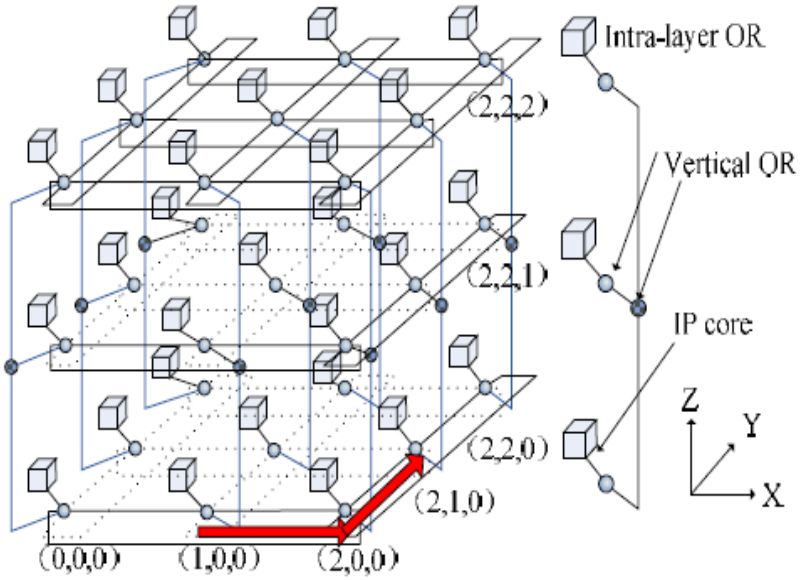

Figure 2: 3D X- Torus Topology

v. Allocator: Its function is to develop switching among input and output channels. Allocator helps to manage interconnection among both channels considering request through particular channel.

Table I: Design Parameters in Router Design

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Vol-22-Issue-16-August-2019

Sr. No.	Parameter Considered	Design Value
1	Switching Technique	Virtual Cut Through (VCT)
2	Number of Virtual Channels	3
3	Packet Width	2048 bits
4	Flow Control	Credit based
5	Link Width	256 bits
6	Design Algorithm	ARA

C
O

IV CONCLUSTION

In NOCs various routing algorithms are proposed and very few of them are implemented in the design architecture. The selection of different routing algorithms is based on network application and its condition. Predestination algorithm, XY routing algorithms are popular algorithms available in NoC Router design. But there are quiet few algorithms available which suits 3D Torus topology which provides researchers scope to develop suitable algorithm for high computing. Virtual Channel (VC) and Virtual Cut through (VCT) switching are used in 3D Torus router design to avoid deadlocks and live locks in the system. Proposed Router design for 3D Torus is efficient in terms of LUTs.

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